CLAIMS

We claim:

1. A wafer-level chip scale package, comprising:

a chip containing a stud bump;

a substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate.

2. The package of claim 1, wherein at least one conductive particle is located between the stud bump and the bond pad.

3. The package of claim 1, wherein the conductive particles comprise metal with an insulating layer.

4. The package of claim 1, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

5. The package of claim 1, wherein the chip contains an integrated circuit in communication with a chip pad.

6. The package of claim 1, wherein the chip contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

7. The package of claim 1, wherein the chip does not contain solder paste.

8. The package of claim 1, wherein the stud bump comprises Cu.

9. The package of claim 8, wherein the stud bump is a coined stud bump.

10. The package of claim 1, wherein the chip does not contain a chip pad overlying an integrated circuit.

11. A wafer-level chip scale package, comprising:

a chip containing a stud bump comprising Cu;

a substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate with at least one conductive particle located between the stud bump and the bond pad.

12. The package of claim 11, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

13. The package of claim 11, wherein the chip contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern

14. The package of claim 11, wherein the chip does not contain solder paste.

15. A packaged semiconductor device, comprising:

a chip containing a stud bump comprising Cu;

a substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate with at least one conductive particle located between the stud bump and the bond pad.

16. The device of claim 15, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

17. The device of claim 15, wherein the chip contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

18. The package of claim 15, wherein the chip does not contain solder paste.

19. An electronic apparatus containing a packaged semiconductor device, the device comprising:

a chip containing a stud bump;

a substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate.

20. A method for making wafer-level chip scale package, comprising:

providing a chip containing a stud bump;

providing a substrate containing a bond pad; and

attaching the chip to the substrate using an adhesive material containing conductive particles.

21. The method of claim 20, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

22. The method of claim 20, including providing the chip with a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

23. The method of claim 20, wherein the chip does not contain solder paste.

24. A method for making wafer-level chip scale package, comprising:

providing a chip with a stud bump;

providing a substrate containing a bond pad

providing an adhesive material containing conductive particles on the chip, the substrate, or both;

pressing the chip and the substrate together; and

curing the adhesive material.

25. The method of claim 24, further comprising providing the chip with a chip pad.

26. The method of claim 24, including providing at least one conductive particle between the stud bump and the bond pad.

27. The method of claim 24, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

28. The method of claim 24, including providing the chip with a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

29. The method of claim 24, wherein the curing the adhesive material attaches the chip to the substrate.

30. The method of claim 29, including attaching the chip to the substrate without solder paste.

31. The method of claim 24, wherein the stud bump comprises Cu.

32. A method for making an electronic apparatus containing a wafer-level chip scale package, the method comprising:

providing a wafer-level chip scale package containing a chip containing a stud bump, a substrate containing a bond pad, and an adhesive material containing conductive particles located between the chip and the substrate; and

mounting the wafer-level chip scale package on a circuit board.